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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|-----------------|-------------|----------------------|---------------------|------------------|
|-----------------|-------------|----------------------|---------------------|------------------|

10/783,789

02/20/2004

Leon Zheng

174/294

7188

36981 7590 07/03/2008

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EXAMINER

DO, CHAT C

ART UNIT

PAPER NUMBER

2193

MAIL DATE

DELIVERY MODE

07/03/2008

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

| | | | |
|------------------------------|--------------------------------------|-------------------------------------|--|
| Office Action Summary | Application No. 10/783,789 | Applicant(s) ZHENG ET AL. | |
| | Examiner CHAT C. DO | Art Unit 2193 | |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 08 May 2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) 11-24 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-10 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This communication is responsive to Amendment filed 05/08/2008.
2. Claims 1-24 are pending in this application. Claims 1 and 8 are independent claims. In Amendment, claims 11-24 are withdrawn from consideration. This Office Action is made non-final after a RCE filed 05/08/2008.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Owen et al. (U.S. 4,876,660).

Re claim 1, Owen et al. disclose in Figure 6A a method for initializing or zeroing an accumulator value (e.g. abstract and Figure 6A) comprising: routing a first pair of input signals (e.g. XA and YA) and a second pair of input signals (e.g. XB and YB) to circuitry that is concentrated in a particular area of a programmable logic resource (e.g. programmable logic 10 in Figure 6A); applying a multiply operation to the second pair of input signals using the circuitry (e.g. first stage with XB*YB as output of multiplier 30); applying a feedback output to the circuitry (e.g. through mux 56), wherein the feedback output is initially set to zero (e.g. as 0 feeding-in); concatenating, in a first clock cycle

(e.g. by clock 1 in Figure 6A), each signal of the first pair of input signals and the feedback output (e.g. second stage with XA and YA are concatenated to form 32-bit into mux 32); and applying an accumulate operation on a result of the multiply operation with a result of the concatenating (e.g. last stage of adder 34 in Figure 6A) in the same first clock cycle (e.g. the feedbacks as accumulation to the adder 34 is capable of adding previous results once the inputs are ready in Figure 6A); and storing a result of the accumulate operation for use as an initialized or zeroed accumulator value (e.g. component 40 or 42 in Figure 6A; Figure 3 and table 4).

Re claim 2, Owen et al. further disclose in Figure 6A setting the first pair of input signals to zero (e.g. by inserting 0 input into mux 32).

Re claim 3, Owen et al. further disclose in Figure 6A applying the accumulate operation comprises one of: adding the result of the multiply operation to the result of the concatenating; and subtracting the result of the multiply operation from the result of the concatenating (e.g. by adder 34 with right side is the result concatenated and the left side is the feedback as the result of multiplication).

Re claim 4, Owen et al. further disclose in Figure 6A setting the first pair of input signals to values that when concatenated in a predetermined order, comprises a first predetermined number of most significant bits of an initialization value (e.g. 32-bits); and setting the second pair of input signals to values such that the result of the multiply operation comprises a second predetermined number of least significant bits of the

initialization value (e.g. both of which can be set to a predetermined number which is zero as feed into mux 32).

Re claim 5, Owen et al. further disclose in Figure 6A the first predetermined number and the second predetermined number comprise the initialization value (e.g. initial zero feed into mux 32).

Re claim 6, Owen et al. further disclose in Figure 6A the feedback output has a number of bits equal to the second predetermined number (e.g. 32-bits).

Re claim 7, Owen et al. further disclose in Figure 6A applying the accumulate operation comprises adding the result of the multiply operation to the result of the concatenating (e.g. the first stage is concatenated of XA and YA; and the second stage is multiplication of $XB*YB$ as reversed).

Re claim 8, Owen et al. disclose in Figure 6A a method for initializing or zeroing an accumulator value (e.g. abstract and Figure 6A) comprising: routing a pair of input signals (e.g. X and Y in registers 14 and 16) to circuitry that is concentrated in a particular area of a programmable logic resource (e.g. programmable logic 10 in Figure 6A); applying a multiply operation to the pair of input signals using the circuitry (e.g. by multiplier 30); clearing a register in the circuitry based on at least one dedicated configuration bit that is set (e.g. setting 0 input into muxes 32 and 56); applying a feedback output to the circuitry (e.g. through mux 56), wherein the feedback output is initially set to zero (e.g. selecting 0 as input to mux 56); concatenating, in a first clock cycle (e.g. by clock 1 in Figure 6A), contents of the register with the feedback output

(e.g. registers 14 and 16 are concatenated to form 32-bit into mux 32); and applying an accumulate operation on a result of the multiply operation with a result of the concatenating (e.g. last stage of adder 34 in Figure 6A) in the same first clock cycle (e.g. the feedbacks as accumulation to the adder 34 is capable of adding previous results once the inputs are ready in Figure 6A); and storing a result of the accumulate operation for use as an initialized or zeroed accumulator value (e.g. component 40 or 42 in Figure 6A; Figure 3 and table 4).

Re claim 9, Owen et al. further disclose in Figure 6A the dedicated configuration bit is set by user input (e.g. all the control signals in Figure 6A for controlling the muxes).

Re claim 10, it has similar limitations cited in claim 3. Thus, claim 10 is also rejected under the same rationale as cited in the rejection of rejected claim 3.

Response to Arguments

5. Applicant's arguments filed 05/08/2008 have been fully considered but they are not persuasive.

a. The applicant argues in page 10 for claims rejected under 35 U.S.C. 102(b) that the cited reference by Owen et al. fails to disclose the newly added limitations of performing any accumulate operation in the same clock cycle as the concatenating step as cited in the claimed invention.

The examiner respectfully submits that the newly added limitations is clearly seen in Figure 6A wherein the series of operations are operated in series/pipeline

manner wherein all the operations are operated at the same time but on different set of data. As seen in Figure 6A, the concatenating is done on the input pair of signals wherein the accumulator is done on the output of the multiplexer 32 (e.g. can be multiplier result) and the feedback of previous result by multiplexer 56.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHAT C. DO whose telephone number is (571)272-3721. The examiner can normally be reached on Tue-Fri 9:00AM to 7:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lewis Bullock can be reached on (571) 272-3759. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.


Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Chat C. Do/
Primary Examiner, Art Unit 2193

July 1, 2008

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| | 10/783,789 | ZHENG ET AL. | |
| | Examiner | Art Unit | |
| | CHAT C. DO | 2193 | |